Power Supply Conditioning Circuit

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This article describes a power supply conditioning circuit that can reduce Periodic And Random Deviations (PARD) on the output voltages of DC power supplies to -150 dBV (32 nanovolts/$\sqrt{Hz}$) from DC to several KHz with no measurable periodic deviations. The PARD for a typical commercial low noise power supply is -74 dBV (200 microvolts/$\sqrt{Hz}$) for frequencies above 20 Hz and is often much worse at frequencies below 20 Hz. The power supply conditioning circuit described in this article relies on the large differences in the dynamic impedances of a constant current diode and a zener diode to establish a DC voltage with low PARD. Power supplies with low PARD are especially important in circuitry involving ultrastable frequencies for the DSN.

I. Introduction

Often DC power supplies are characterized by the PARD on their output voltages. The PARD is the periodic and random deviation of a DC voltage or current from its average value, over a specified bandwidth, with all influence and control quantities maintained constant. A bandwidth commonly used to specify PARD is 20 Hz to 20 MHz.

The PARD on the output voltage of a power supply used to power RF circuitry results in undesired amplitude and phase modulation of the RF signal being processed or generated. This problem is especially significant when using ultrastable frequencies generated by modern atomic frequency standards (e.g., σ_y [100 seconds] = 8.5×10^{-13} for cesium). In order to minimize the spurious AM and PM modulation of ultrastable frequencies, the PARD on the associated power supply voltages must be minimized. Most commercial power supplies do not reduce the periodic variations, predominately at 60 Hz and its harmonics, to a low enough level to use in ultrastable RF circuitry. These periodic variations should be reduced below the level of random deviation (noise). The need for a power supply conditioner came about when the phase noise of a low noise voltage controlled oscillator was measured and found to exceed the specification for spurious signals. It was determined that PARD from the power supply was modulating the RF output signal.

Sidebands that are generated in frequency multiplier circuits as a result of PARD on the power supply voltage are of particular concern because the power in sidebands, P_{sb}, is increased by,

$$P_{sb} = 20 \log (f_2/f_1) \quad (1)$$

where f_1 is the input frequency and f_2 is the output frequency of the multiplier. For example, if a 5 MHz reference frequency is multiplied to 10 GHz the sidebands will increase by 66 dB. This increase in sideband power will often degrade the stability of the desired high frequency signal to an unacceptable level.

The power supply conditioning circuit described in this article takes advantage of the large difference in dynamic impedance of constant current diodes and low voltage avalanche zener diodes. This design uses the reference voltage established by a constant current diode and a zener diode to generate a DC output voltage with low PARD.

II. Design

The circuit in Fig. 1 is capable of providing a DC reference voltage having extremely low PARD for frequencies ranging from DC to several KHz. The constant current diode (D_1) and zener diode (D_2) in series form a voltage divider having a very large division ratio for AC signals. Using the voltage divider equation, the deviation, e_o, of the output voltage caused by a deviation in the input voltage, e_i, will be,

$$e_o = \frac{r_z}{r_c + r_z} e_i \qquad (2)$$

where

r_z = dynamic impedance of the zener diode, and

r_c = dynamic impedance of the constant current diode.

The dynamic impedance of the constant current diode can be greater than 100 Kohms and the dynamic impedance of the zener diode can be less than 10 ohms. If Eq. (1) is evaluated for r_c = 100 Kohms and r_z = 10 ohms the rejection ratio, e_o/e_i, will be 10^{-4} or -80 dB. Thus, the large dynamic impedance of the constant current diode and the small dynamic impedance of the zener diode, cause any deviation of the DC voltage applied to the input of the voltage reference circuit to be greatly reduced at the output of the circuit.

For the best results this circuit requires the use of a constant current diode with the highest possible dynamic impedance and a zener diode with the lowest possible dynamic impedance. [1]. However, certain compromises must be made in designing the circuit. The dynamic impedances of constant current diodes have an inverse relationship to the current rating. As the current ratings of constant current diodes go down, the dynamic impedances go up. This makes it necessary to use a zener diode which is designed to have a low impedance at a low current so that the highest possible impedance ratio consistent with good zener regulation can be obtained. Low voltage avalanche zener diodes meet this requirement and have low noise as well.

Since one of the requirements for achieving a maximum rejection ratio in this circuit is to use the lowest possible current, this circuit can only be used as a voltage reference. The design described below uses additional circuitry to maintain an output voltage with low PARD and to increase the output current.

In the field effect transistor (FET) circuit (Fig. 2), the reference is reproduced at the output using feedback. An operational amplifier (op amp), U_1, used in conjunction with a field effect transistor, Q_1, increases the current capability. The output voltage of the op amp controls the current through Q_1 in such a manner as to reproduce the reference voltage at the circuit output. Fluctuations on the drain voltage are not reproduced at the source due to the high impedance between the drain and source.

For most applications the rejection ratio provided by this circuit is sufficient, but if even more rejection is required, the rejection ratio can be increased by connecting two stages in series (Fig. 3).

III. Small Signal Analysis

A theoretical rejection ratio for this circuit can be determined using a small signal analysis. This analysis illustrates which parameters limit the performance of the circuit. Input PARD is represented by an AC voltage source. Superposition may be used to determine the effect of this source, by applying the source to different points in the model. In this case, the AC source is first applied to the anode of the constant current diode and then to the drain of the FET (Figs. 4. and 5).

The rejection ratios are defined in dB to be

$$Rr_1 = 20 \log \left[\frac{Vout_1}{Vin}\right] \qquad (3)$$

$$Rr_2 = 20 \log \left[\frac{Vout_2}{Vin}\right] \qquad (4)$$

and

$$Rr_t = 20 \log \left[10 \exp \left(\frac{Rr_1}{20}\right) + 10 \exp \left(\frac{Rr_2}{20}\right)\right] \qquad (5)$$

where

Rr_1 = rejection ratio with the AC source connected to the anode of the constant current diode,

Rr_2 = rejection ratio with the AC source connected to the drain of the FET,

Rr_t = total rejection ratio,

$V\text{out}_1$ = AC output voltage with the AC source connected to the anode of the constant current diode,

$V\text{out}_2$ = AC output voltage with the AC source connected to the drain of the FET,

$V\text{in}$ = AC input voltage.

As shown in Eq. (5), the overall rejection ratio of this circuit is approximately equal to the poorer of the two independent rejection ratios.

IV. Analysis of FET Circuit

For purposes of analysis, the FET circuit was simplified by removing the bypass capacitor. The analysis of the model (Fig. 4) with the AC source connected to the anode of the constant current diode, shows this rejection ratio to be largely determined by the dynamic impedances of the constant current diode and the zener diode. The following equations may be arrived at from the model [2].

$$\frac{V_2 - V\text{in}}{R_c} + \frac{V_2}{R_z} + \frac{V_2 - V\text{out}_1}{R_{in}} = 0 \qquad (6)$$

$$\frac{V\text{out}_1 - V_2}{R_{in}} = g_m Vgs - \frac{V\text{out}_1}{R_{eq}} \qquad (7)$$

$$Vg = A\,(V_2 - V\text{out}_1) \qquad (8)$$

$$Vs = V\text{out}_1 \qquad (9)$$

$$Vgs = AV_2 - (A+1)\,V\text{out}_1 \qquad (10)$$

where

R_{in} = input impedance of operational amplifier

R_{out} = output impedance of operational amplifier

A = gain of operational amplifier

$R_{eq} = R_{ld}//R_o$

R_{ld} = load resistance

R_o = drain source resistance

Vg = AC gate voltage

Vs = AC source voltage

Vgs = AC gate to source voltage

g_m = transconductance of the MOSFET

In the above, as well as throughout the remainder of this article, the symbol $R_1//R_2$ represents the lumped resistance due to R_1 and R_2 being in parallel. In other words

$$R_1//R_2 = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}}$$

Combining Eqs. (6), (7), and (10) leads to

$$\frac{V\text{out}_1}{V\text{in}} = \frac{R_{eq}(R_a)(1 + g_m A R_{in})}{R_c\left[R_{eq} + R_{in} + g_m R_{in} R_{eq}(A+1) - \left(\frac{1}{R_{in}} + g_m A\right) R_{eq}(R_a)\right]} \qquad (11)$$

where $R_a = R_c//R_z//R_{in}$

With the assumptions

$$A \gg 1$$

$$R_c \gg R_z$$

$$R_{in} \gg R_z$$

$$R_o \gg R_{ld}$$

Eq. (11) reduces to

$$\frac{V\text{out}_1}{V\text{in}} = \frac{R_z}{R_c} \qquad (12)$$

The analysis of the model (Fig. 5) with the AC source connected to the drain of the MOSFET shows this rejection ratio to be largely determined by the transconductance and drain to source resistance of the MOSFET, and the gain of the op amp. The following equations may be derived from the model.

$$\frac{V\text{out}_2}{R_{ld}} + \frac{V\text{out}_2}{(R_c//R_z) + R_{in}} = g_m Vgs + \frac{V\text{in} - V\text{out}_2}{R_o} \qquad (13)$$

$$\frac{V_2}{R_c} + \frac{V_2}{R_z} = \frac{V\text{out}_2 - V_2}{R_{in}} \tag{14}$$

$$Vg = A\,(V_2 - V\text{out}_2) \tag{15}$$

$$Vs = V\text{out}_2 \tag{16}$$

$$Vgs = AV_2 - (A+1)\,V\text{out}_2 \tag{17}$$

Combining Eqs. (13), (14), and (17) leads to

$$\frac{V\text{out}_2}{V\text{in}} = \frac{\frac{1}{R_o}}{\frac{1}{R_{ld}} + \frac{1}{R_b} + \frac{1}{R_o} + g_m(A+1) - \frac{g_m A(R_a)}{R_{in}}} \tag{18}$$

where

$$R_a = R_c//R_z//R_{in}$$

and

$$R_b = (R_c//R_z) + R_{in}$$

With the assumptions

$$A \gg 1$$

$$R_c \gg R_z$$

$$R_{in} \gg R_z$$

$$R_o \gg 1$$

$$R_{ld} > 1$$

Eq. (18) reduces to

$$\frac{V\text{out}_2}{V\text{in}} = \frac{1}{g_m A R_o} \tag{19}$$

A component listing for an FET circuit (Fig. 6) that was tested is given below.

D_1	1N5314	4.7 mA constant current diode
D_2, D_3, D_4	LVA351A	5.1 V zener diode
U_1	OP-27	Low noise precision op amp (PMI)
Q_1	VN88AF	N-channel enhancement MOSFET
R_x		1 Kohm resistor
R_{ld}		30 ohm resistor
C_1		1uF capacitor

The rejection ratio of this circuit was determined by adding an AC voltage to the DC supply and measuring the AC voltage present at the output of the power supply conditioner. A -10 dBV AC signal was added to the input and rejection ratios near -70 dB were measured for frequencies ranging from 1 Hz to 10 KHz (Fig. 7). The input voltage was 22.0 V and the output voltage 15.3 V, with an output current of 0.5A.

Equations (12) and (19) were used to compare this result with the theoretical results, using values

$A = 10^{-6}$

$g_m = 195 \times 10^{-3}$ siemens

$R_o = 3$ Kohms

$R_c = 50$ Kohms

$R_z = 15$ ohms

The theoretical rejection ratio due to the constant current diode and the zener diode is -70 dB, while that due to the MOSFET is -175 dB. Thus in this case, the dynamic impedances of the constant current zener diodes limit the rejection ratio to -70 dB.

V. Conclusion

The power supply conditioner described above provides a simple and effective way to reduce the PARD found on the output voltages of power supplies. A low noise voltage reference, consisting of a constant current diode and a low noise zener diode connected in series, provides the basis for this design. The rejection ratio of this design is determined by the ratio of the dynamic impedances of the constant current diode and the zener diode, and can be improved by increasing this ratio and using lower noise zener diodes. Further improvements can be made by connecting two stages in series. An additional advantage of this power supply conditioner is that it provides large current capabilities, making it a practical addition to systems requiring power supplies with low PARD down to DC.

References

[1] G. F. Lutes, "Stable Low Noise Voltage Source," *JPL DSN Progress Report 42-47*, vol. July and August 1978, pp. 89-93, Jet Propulsion Laboratory, Pasadena, Calif., Oct. 15, 1978.

[2] R. A. Colclaser, D. A. Neamen, and C. F. Hawkins, *Electronic Circuit Analysis Basic Principles*, John Wiley & Sons, Inc., USA, pp. 339-392, 1984.

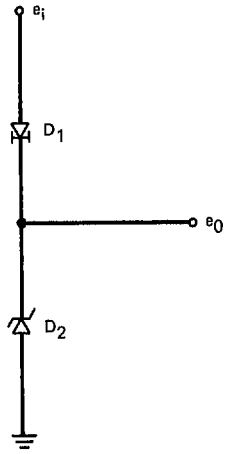

Fig. 1. Voltage reference circuit

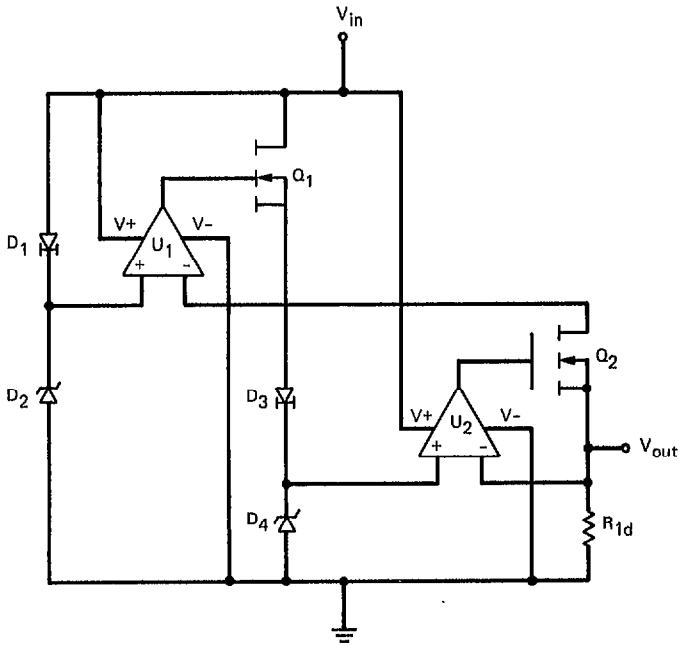

Fig. 3. Two staged FET circuit

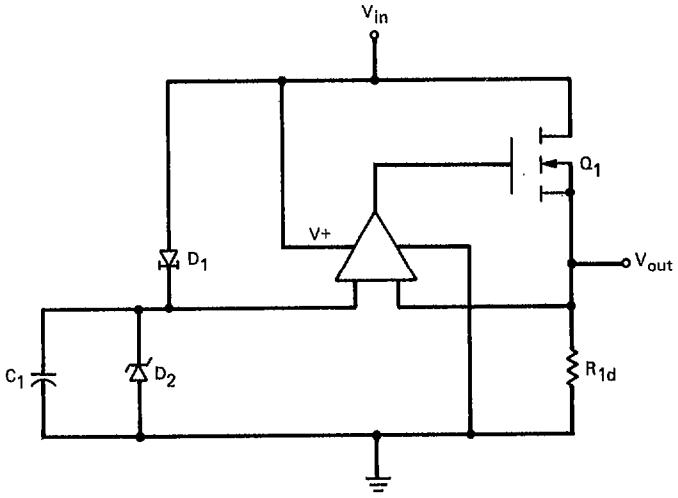

Fig. 2. FET circuit

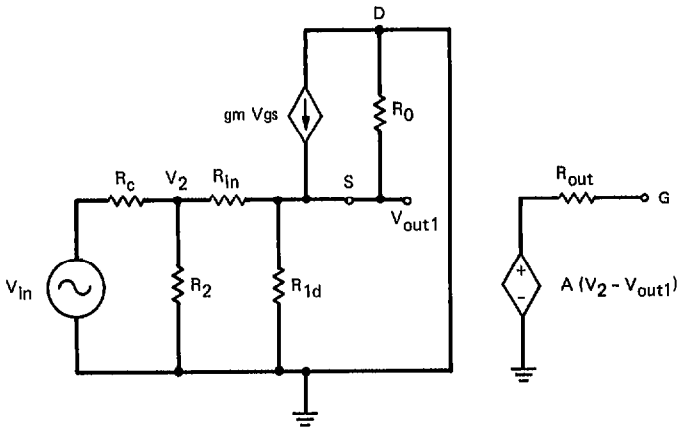

Fig. 4. Small signal model with AC source on anode of constant diode (Rc)

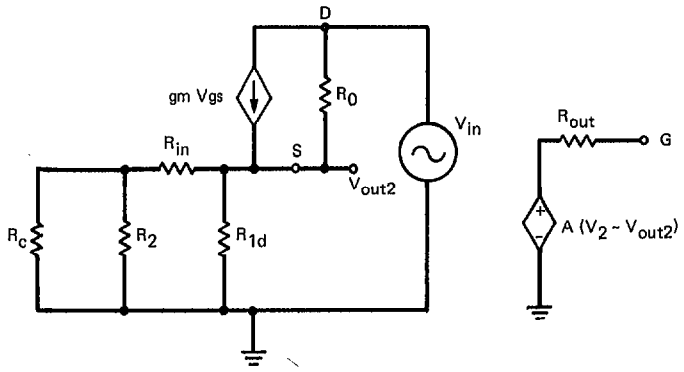

Fig. 5. Small signal model with AC source on drain of FET

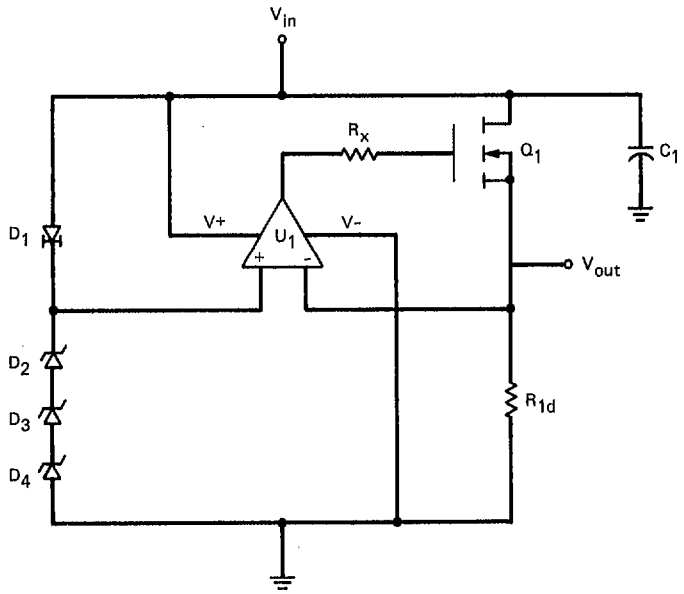

Fig. 6. Example FET circuit

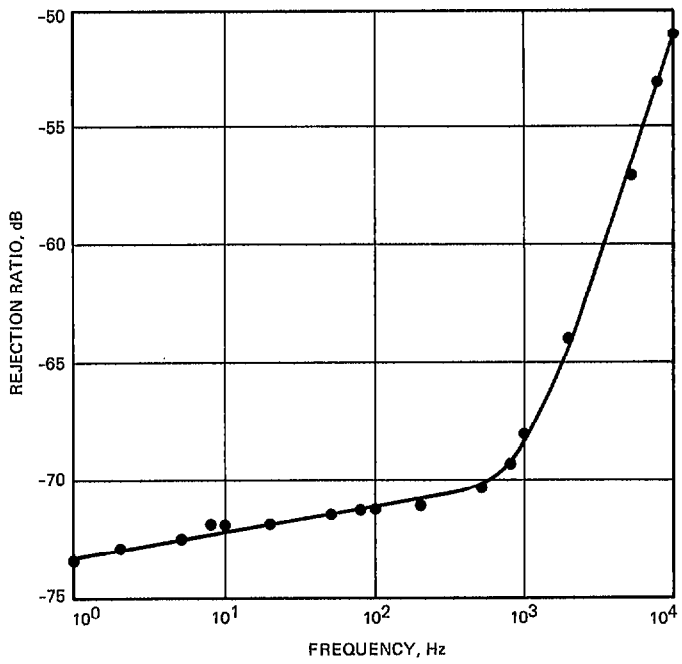

Fig. 7. Measured rejection ratio vs. frequency for FET circuit